RTL/Frontend Design Engineer

Flex Logix develops industry-leading AI inference engines and we are the #1 provider of eFPGA solutions. Our InferX X1 is the industry's fastest and most-efficient AI edge inference accelerator that brings AI to high-volume applications, surpassing competitor's performance at 1/7th size and much lower price. InferX X1 is available as a chip, PCIe board and M.2 board. InferX X1 is working and running YOLOv3 today and starts production shipments in 2022. Our Inference Compiler is easy to use (we take in neural network models in TensorFlowLite and ONNX) and our APIs for Infer X1 allow rapid integration by the customer. Our architecture is covered by dozens of patents and is highly differentiated giving us a sustainable competitive advantage.

We recently completed a $55M funding round.

Flex Logix is seeking a RTL/Frontend Design Engineer to join our team developing/migrating the RTL of the eFPGA and the next-generation InferX solutions.

RESPONSIBILITIES

The candidate must be able to work in the architecture/frontend stage of silicon development: specification, coding, some verification, and some synthesis support for the

- Flex-Logix in-house interconnect switch/bitcell modeling
- eFPGA reconfigurable building block (RBB), block memory (BRAM), and IP netlist
- InferX reconfigurable tensor processor block
- InferX high-speed configurator
- MBIST/Repair RTL generation for memory IPs

EXPERIENCE AND SKILL REQUIRED

- BS/MSEE/CE/CS with a minimum of 3 years of experience in RTL design or functional verification
- Experience with starting designs from scratch
- Extensive experience coding Verilog, running simulation, and debugging simulation failure
- Experience interfacing with internal and 3rd party IP suppliers
- Experience running Lint, CDC, and other static quality checks
- Working knowledge of System Verilog
- Experience scripting in Python or Perl
- Work effectively with verification team to deliver a high-quality RTL which is easy to maintain, scalable, and with high-speed performance
- Must be passionate about doing this job: wanting to change the world and work hard doing it
- Must be entrepreneurial in spirit and an innovative problem solver

Preferred or willing to learn:

- Knowledge of computer architecture, especially in systolic arrays
- Familiarity with memory architecture in SoCs
- Experience with DDR and PCIe standards
- Experience with FPGA design and emulation
- Experience with FPGA and ASIC EDA tools
- Experience interfacing with back-end teams (silicon engineering)
- Familiarity with C or C++ coding
- Experience with DMA, DDR controllers, NoC configuration, and other 3rd party IP
- Logic/physical synthesis of RTL

MUST live in Silicon Valley or Austin TX and have a US citizenship or permanent residency (“green card”), or holding a current H1-B visa