Physical Design Engineer (Entry/Senior/Principal)

Flex Logix develops industry-leading AI inference engines and we are the #1 provider of eFPGA solutions. Our InferX X1 is the industry's fastest and most-efficient AI edge inference accelerator that brings AI to high-volume applications, surpassing competitor's performance at 1/7th size and much lower price. InferX X1 is available as a chip, PCIe board and M.2 board. InferX X1 is working and running YOLOv3 as well as other models today and is ready for production. Our Inference Compiler is easy to use (we take in neural network models in TensorFlowLite and ONNX) and our APIs for Infer X1 allow rapid integration by the customer. Our architecture is covered by dozens of patents and is highly differentiated giving us a sustainable competitive advantage.

We recently completed a $55M funding round.

Qualification

- The ideal candidate will have at least 5+ years of Physical Design experience on IP and/or SOC designs: your title will be based on your current level and experience
- Deep Knowledge about industry standards and practices in Physical Design, including Physically aware synthesis, Floor-planning, and Place & Route
- Experience in developing and implementing Power-grid and Clock specifications
- Strong understanding of all aspects of Physical construction, Integration and Physical Verification
- Shown Knowledge of Basic SoC Architecture and HDL languages like Verilog to be able to work with logic design team for timing fixes
- Power user of industry standard Physical Design & Synthesis tools.
- Familiar with power intent definition, implementation and verification flows.
- Familiar with of power analysis and optimization methods.
- Deep Understanding of scripting languages such as Perl/Tcl, solid understanding of Extraction and STA methodology and tools
- Deep Understanding of Physical Design Verification methodology to debug LVS/DRC issues at chip/block level
- Bachelors or Master's Degree in EE/CS required

Primary Responsibilities:

- Your responsibilities include but are not limited to: Generate block/chip level static timing constraints
- Build full chip/IP floor-plan including pin placement, partitions and power grid
- Develop and validate high performance low power clock network guidelines
- Perform block level place and route and close the design to meet timing, area and power constraints
- Generate and Implement ECOs to fix timing, noise and EM IR violations
- Run Physical design verification flow at chip/block level and provide guidelines to fix LVS/DRC violations to other designers

- Participate in establishing CAD and physical design methodologies for correct by construction designs

Must be passionate about being part of an aggressive, venture-backed startup team that is changing chip architecture. Must be entrepreneurial, innovative problem solver and willing to work hard.

Must live in Silicon Valley or Austin area and have US citizenship or permanent residency (“green card”), or holding a current H1-B visa