Sr. eFPGA EDA Static Timing Software Engineer

Flex Logix is developing industry-leading AI inference engines and we are the #1 provider of eFPGA solutions. Our InferX X1 is the industry's fastest and most-efficient AI edge inference accelerator that will bring AI to the masses in high-volume applications, surpassing competitor's performance at 1/7th size and much lower price. InferX X1 is available as a chip, PCIe board and M.2 board. InferX X1 is working and running YOLOv3 today; we launched it at the Linley 2020 Fall Processor Conference. Our Inference Compiler is easy to use and our APIs for Infer X1 allow rapid integration by the customer. Production shipment and compiler availability commences mid-2021. Our architecture is covered by dozens of patents and is highly differentiated giving us a sustainable competitive advantage.

We recently completed a $55M funding round.

RESPONSIBILITIES

The Flex-Logix EFLX eFPGA architecture supports a proprietary AI inference engine (InferX) and eFPGA designs up to 500k LUTs with future support to 1M LUTs.

As a member of our placement & routing team, you will contribute to the development of a best-in-class placement and routing tool for eFPGAs.

In this role you will develop a static timing analysis engine (STA). You will Also define eFPGA timing models for a new eFPGA placement and routing system.

PREFERRED SKILLS (FPGA or ASIC)

- Static timing analysis (STA)
- Incremental static timing analysis
- Multi-Mode and Multi-Corner timing analysis
- Synopsys Design Constraints (SDC)
- Placement optimization
- Timing driven placement and routing
- Multi-threaded algorithm development
- FPGA experience

EXPERIENCE AND SKILL REQUIRED

BS/MS/PhD Computer Science, or equivalent, with 5+ years of relevant industry experience.

Must have EDA development experience (FPGA/ASIC/SOC) in static timing analysis.

Must have 5+ years of strong C++ development experience.

Must have 2+ years of Tcl development experience.

Must have solid foundation in data-structures, algorithm development and algorithmic complexity.

Must be passionate about being part of an aggressive, venture-backed startup that is changing chip architecture. Ability to work independently. Must be entrepreneurial, innovative problem solver and willing to work hard.

Work location is either Mt. View, California or Austin, Texas

Must have US citizenship or permanent residency or a current H1-B visa.

Occasional travel will be required.